Q.P. Code: 16CS506 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Supplementary Examinations August-2022

DIGITAL LOGIC DESIGN

(Common to CSE & CSIT)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Represent the decimal number 3452 in i)BCD ii)Hexadecimal and iii)perform (-50)-(-10) in binary using the signed-2's complement	**6M**
	b	Simplify the Boolean expressions to minimum number of literals i) **(**A + B)(A + C')(B' + C') **ii)** AB + (AC)' + AB'C(AB + C)	**6M**

OR

2	**a**	Explain the Binary codes with examples.	**6M**
	b	Simplify the Boolean expressions to minimum number of literals i) X' + XY + X Z' + XYZ' ii) (X+Y) (X+Y')	**6M**

UNIT-II

3	**a**	Simplify the Boolean expression using K-map and implement using NAND gates F(A,B,C,D) = ∑m(0,2,3,8,10,11,12,14)	**6M**
	b	Explain NAND- NOR implementations.	**6M**

OR

4	**a**	Design the circuit by Using NAND gates F= ABC'+ DE+ AB'D'	**6M**
	b	Design the circuit by Using NOR gates F= (X+Y). (X'+Y'+Z')	**6M**

UNIT-III

5	**a**	Explain Carry Lookahead Generator.	**6M**
	b	Implement the following Boolean function using 8:1 multiplexer F(A, B, C, D) = A'BD' + ACD + A'C' D +B'CD	**6M**

OR

6	**a**	Explain Full binary subtractor in detail.	**6M**
	b	Define Full Adder and explain the operations of Full Adder.	**6M**

UNIT-IV

7	**a**	Explain the Logic diagram of JK flip-flop.	**6M**
	b	Write difference between Combinational & Sequential circuits.	**6M**

OR

8	**a**	Draw and explain the operation of T Flip-Flop.	**6M**
	b	Explain the Ring counter.	**6M**

UNIT-V

9	**a**	Compare between PROM, PLA &PAL.	**6M**
	b	Explain about Error correction & Detection Codes.	**6M**

OR

10	**a**	Implement the following function using PLA A(x,y,z)=∑m(1,2,4,6) B(x,y,z)=∑m(0,1,6,7) C(x,y,z)=∑m(2,6)	**6M**
	b	Explain about Hamming Code with example.	**6M**

*** END ***